Testing Of Digital Circuits with Conserved Power Utilization: Jumbled Test Sequence Approach

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Abstract--Reduction of power dissipation during combinational circuit testing can be a challenging task in VLSI circuits. This is accomplished by jumbling up the evaluation vector application sequence so that the current collection gives less changing activity during testing. This subsequently reduces the power dissipation of the Circuit Under Test (CUT). Jumbled test sequence approach is applied utilizing Graph Theory concept. Testing power is reduced by this algorithm without affecting the fault coverage. Fresh outcome of the proposed algorithm with ISCAS85 benchmark circuits reveal the switching activity might be decreased up to 72 times when compared to the previous research paper of this work and existing work.

Index Terms: ATPG, Hamming Distance, Switching Activity, Reordering, Power Consumption

1. INTRODUCTION

Lately, energy usage and power dissipation have attained substantial focus in VLSI circuit design. Several factors have led to this trend. With the arrival of mobile products, low energy consumption has become one of many leading design goals in order to lengthen battery life. Moreover the amount of energy consumed by the circuit is directly reflected in its heat dissipation, and requires costly packaging and chilling practices, which raises system cost [9]. Additionally, as power consumption increases, signal reliability gets impacted negatively because of electro migration. When the circuit is examined with pseudorandom patterns, successive input test vectors are statistically separate which leads to increased switching activity within the signal under test. The average power usage during screening is considerably greater than normal way of operation, because in CMOS circuits energy is mostly consumed by signal changeover. The earlier work of this paper was based in the Hamming Distance between two successive test vectors. The test vectors are reordered so that the complete hamming distance for that entire test set is minimal. This Hamming Distance approach is dependent on the notion the internal switching activity is more or less depending in the distance at the feedback of the signal. This theory isn't accurate for all the circuits and also the switching activity is depending on the logic gates which are utilized to assemble the circuit. In this paper a new method is suggested in which changing action of the routine is considered rather hamming Space for reordering of test vectors. The test energy obtained by utilizing the reordered test set is seen as ideal test strength.

More methods are mentioned in literature for reducing testing ability. From which two procedures were proposed in [6] and [7] to decrease testing power using changing task concept.

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Both the strategies are derived from Genetic Algorithm approach in which the fault coverage is transformed while reordering is carried out. This will definitely degrade the operation of fault simulator algorithm or Automatic Test Pattern Generator (ATPG).The proposed method is dependent upon Graph Theory method where the fault coverage isn't transformed and important improvement in minimizing switching activity during screening is realized.

2. POWER DISSIPATION IN CMOS TECHNOLOGY

The Power dissipation in CMOS technology [8,10] can be classified into static and dynamic. Fixed dissipation is because of leakage current that has small magnitude in digital CMOS circuits. Therefore, for such circuits, the powerful dissipation is the dominant term. Energetic dissipation occurs in a node once it switches from one logic level to some other logic stage. Dynamic dissipation is broken into two parts caused by charge / discharge current and short-circuits current. The later is caused by switching activity of transistors during $0 \to 1$ or from $1 \to 0$ transitions. The charge/discharge present is the present that charges and discharges the capacitive load on the production of a gate during $0 \to 1$ or from $1 \to 0$ transitions and in common, dominates energetic power dissipation [10,3]. The dynamic power dissipation (PD) in the route is given by (1)

$$PD = \frac{1}{2} \sum jn \, C_L(j) s(j) V_{dd}^{\,2} \quad (1)$$

where $C_L(j)$ is the load capacitance at line j of the Circuit Under Test (CUT), $s(j)$ is the regularity of switching of the line j, and V_{dd} is the power Supply voltage. Other quantities organism constant for a given course, test vector set generated

to diminish the frequency of control at circuit lines during test submission will minimize the heat debauchery during testing.

In this thesis we present a new method for power reduction in testing of digital circuits

3. PROBLEM FORMULATION AND JUMBLED TEST SEQUENCE APPROACH

The power dissipation during testing [4] is minimized by lowering the number of transition in the circuit. Generally test vectors come in arbitrary and thus it is needed so the switching action between consecutive test vectors is minimal to arrange the sequence of incidence of test vectors.

The problem of minimizing switching power is solved by data theory using Hamiltonian path [5] method. The problem is formulated by contemplating the evaluation vector as node and changing activity between them as border expense of the chart. Here the Hamiltonian path is really a path with minimal total edge cost and all nodes. Reordering formula [1] is used to assemble the Hamiltonian path, which is resultant reordered test vector set whose absolute switching activity is minimum. Now the path developed from the algorithm is reordered test vector series which offers less number of transitions in the routine which subsequently leads to decreased power dissipation in the Circuit Under Test (CUT) throughout screening [5]. The Algorithm to decrease the Switching activity during testing is following.

1. Mull over a digital circuit with p inputs and q outputs.

2. Generate all the test vectors to observe the entire single stuck at faults [4] of the course. The analysis vector may be having don't care. Let the digit of test vectors be n.

3. Find the internal switching action between each and every test vector by affect them in the CUT and load the identical in array swa of size n x n. Let $\mathrm{swa}[\mathrm{i}][\mathrm{j}]$ be the array component that gives switching movement between i^{th} and j^{th} test vector.

4. Find the internal switching movement of every test vector by applying them in the CUT independently and load the same in array $\mathrm{swa\_init}$ of size $\mathrm{n\ x\ 1}$. Let $\mathrm{swa\_init}[\mathrm{i}]$ be the array component that gives initial switching activity when i^{th} test vector is applied.

5. Apply reordering algorithm to find the reordered test vector succession with minimum total switching activity.

3.1. Jumbled Test Sequence Approach:

The various parameters used in the algorithms are as follows:

$t_1, t_2, \ldots t_n$, be n test vectors with m bits each.

$\mathrm{T} = \{1, 2, .\ \mathrm{k} \ldots \mathrm{n}\}$, where k represents k^{th} position in the vector set generated.

R, is a set to store prepared test vector sequence.

Q is a set to store $\mathrm{T} - \mathrm{R}$.

Step 1: Select a test vector x such that $\mathrm{swa\_init}[\mathrm{x}]$ is minimum. Add x to set R.

Step 2: Select a test vector $Y_{\min}$ such that $\mathrm{swa}[x][y_{\min}]$ is minimum.

Step 3: Add $Y_{\min}$ to R. $Q \to T - R$. $X_{\min} \leftarrow Y_{\min}$.

Step 4: From $\mathrm{swa}\,[X_{\min}][\mathrm{j}]$ where j varies as in Q, find minimum value as $\mathrm{swa}\,[X_{\min}][Y_{\min}]$. Go to step 3.

Step 5: If Q is not empty go to step 3 otherwise go to step 6.

Step 6: Stop the process and find the total switching movement of the circuit.

Finally set R will have reordered test vector succession with minimum switching movement in the CUT. When the reordered test vectors are practical the total switching activity of the circuit is designed by the given equation,

$$SWA_{total} = swa\_init[R[1]] + \sum_{i=1}^{n-1} swa[R[i]][Ri+1]$$

Where n = total number of test vectors.

$\mathrm{R}[\mathrm{i}] = \mathrm{i}^{\mathrm{th}}$ positional test vector number stored in the set R.

The aforementioned procedure is illustrated with simple $\mathrm{ISCAS85}$ benchmark circuit $\mathrm{c17}$ to show the effectiveness of the suggested system. The test vector set that employed to detect the whole single stuck at faults is given in Table 1. This is created by ATPG tool called ATALANTA. The vectors are displayed by the sequence of incident for the interest of convenience. The switching activity arrays $\mathrm{swa}\,[\,]\,[\,]$ and $\mathrm{swa\_init}\,[\,]$ are constructed by using the evaluation set in CUT. This is provided as in (2) and (3). On application of reordering algorithm to these matrices, the reordered test vectors sequence is created with minimum switching action.

Table.1 Test vectors for c17 circuit

Test vector set (n=6)	No.
11100	t1
11111	t2
00000	t3
01110	t4
01011	t5
10001	t6

$$swa[i][j] =$$
$$\{[(t1,t2)=7,(t1,t3)=7,(t1,t4)=7,(t1,t5)=6,(t1,t6)=7]$$
$$[(t2,t1)=5,(t2,t3)=8,(t2,t4)=4,(t2,t5)=9,(t2,t6)=8]$$
$$[(t3,t1)=7,(t3,t2)=14,(t3,t4)=10,(t3,t5)=7,(t3,t6)=4]$$
$$[(t4,t1)=7,(t4,t2)=4,(t4,t3)=4,(t4,t5)=7,(t4,t6)=8]$$
$$[(t5,t1)=6,(t5,t2)=7,(t5,t3)=7,(t5,t4)=7,(t5,t6)=5]$$
$$[(t6,t1)=7,(t6,t2)=10,(t6,t3)=4,(t6,t4)=12,(t6,t5)=5]\}$$

$$swa\_init[i] =$$
$$[t1=15,t2=22,t3=0,t4=18,t5=15,t6=12]$$

After applying the test sequence jumbling approach, the jumbled test sequence is specified as t3 - t6 - t5 - t1 - t2 - t4 whose total switching movement is 26. The proposed method reduces the switching activity from original value 49 to final value 26, which shows that 47% of decrease in switching activity is attained

4. RESULTS AND DISCUSSIONS

The algorithm is examined and employed with ISCAS 85 benchmark circuits. The results are shown within the Table 2 for the proposed work and its previous work which was centered on switching activity [11]. For every single circuit, an array of test vectors to detect single stuck at faults are created. Total switching activity is calculated for every single test vector and also the switching activity matrix is obtained. The switching action matrix is placed on the reordering algorithm. The total switching action of the routine after reordering is shown in the "projected work" by $swa[i][j]$. The effects of projected work are compared with previous work [2] [11] and their percent improvement is shown in last two columns of the resultant table. The results shown in these experiments are that switching activity is reduced up to 72% for the benchmark circuit $c1355$. Thus the reduction in switching task reduces the testing power in combinational circuit.

5. CONCLUSION

Within this paper a strategy is proposed for decreasing the power dissipation during testing of combinational circuit. The proposed jumbled test sequence approach algorithm lessens the switching activity by reordering the test vectors, since the 80% of the complete power dissipation in CMOS circuits is a result of the switching activity. The algorithm is created using graph theory model and implemented by C language and Hardware Description Language (HDL) simulation programs. The functionality of the algorithm is tested with ISCAS bench mark circuits. Experimental results demonstrate that new approach reduces switching activity up to 72% when the test vectors generated by the proposed algorithm are utilized during test phase. Thus there's a decrease in power dissipation during test phase. The low power design in VLSI Circuits make real demands for the test power optimization approaches of better optimization effect and time saving.

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